Interconnect Technique for Tight Clearance in Stacked-die Package

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Authors’ contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

The paper focused in addressing wire-related assembly issues due to tight clearances in the semiconductor package design. Package design characterization was done considering the assembly design rules and the advanced rules, resulting to the integration of an interposer in the package design. With the new design, the assembly limitations and capability could be improved specifically for semiconductor devices with tight clearance requirement. Furthermore, gross assembly rejections related to tight clearances could be mitigated with the design solution and process improvement.

Keywords: Stacked dice; wirebonding; semiconductor; interposer; wire short.

1. INTRODUCTION

The down-scaling of integrated circuit (IC) device has become the common direction for semiconductor IC industry, converting the device into smaller size yet with increased number of functional components. Aligned with this common goal is to continuously improve the manufacturing and assembly side of semiconductor devices as well to be able to adapt to the fast changing requirement of technological breakthrough. Tight clearance in a
A cross-sectional view of a semiconductor package with stacked-die configuration in Fig. 1 shows a critical location where tight clearance is identified. In this scenario, risk of assembly rejection is manifested especially during wirebond interconnect (or simply wirebonding) process wherein the wiring from the top die (or Die 2) and bond fingers connection becomes electrically shorted.

Another assembly reject that may occur due to tight clearances is the shorting between wires as seen in Fig. 2. This occurrence is closely monitored as it is considered a hard reject, affecting the functionality of the device. It is imperative that assembly rejects be eliminated to ensure the product quality. Note that criteria for assembly rejects and visual inspection are governed by internal specifications and work instruction documents [4,5].

Careful analysis of the problem leads to isolate that the occurrence of the wire shorting is evident only on circumstances that the placement of Die 2 is offset near to the bond finger location. Succeeding evaluation clearly identified two assembly challenges related to this device: (1) first is the wirebonding integrity for smaller/tight clearances, (2) placement deviation during die attach process.

2. LITERATURE REVIEW AND DESIGN SOLUTION

A semiconductor package solution with improved interconnect technique through integrating an interposer design is presented in this paper to improve the packaging strategy of IC technology and provide reliable options for miniaturization requirement.

2.1 Packaging Design

An isometric view of the improved semiconductor package design in Fig. 3 illustrates the location of the components inside the package.

The interposer is incorporated in the bond finger part elevating the connection of the leads up to the height of the top die. The bottom part of the interposer is electrically connected to the bond fingers while the topside portion of the interposer is designed to have bondable pads for the wiring and connection of the top die. The number of die stack-up could be more than two however the height of the interposer should be adjusted as well.

2.2 Interposer Design

The interposer is the extension of the electrical layering of the substrate when it is attached to the bond fingers. The innermost connection or the through via hole will be filled with a conductive material for electrical connection. However, if a non-conductive fill or material is used for the filling, the copper boundary or wall as shown in Fig. 4 should still be connected to bottom connection of the interposer.

The topside portion or the bond pad of the interposer is designed to be bondable for the wiring material. A cost-effective candidate for the bond pad of the interposer is a copper material with the exposed portion can be coated with flash of gold for good inter metallic response between the wiring materials.
A ceramic or polymer material could be used to isolate the conductive part of the interposer to the neighboring electrical components. In addition, this provide stability also for the interposer to avoid sagging or breaking during the assembly.

3. METHODOLOGY

3.1 Assembly Process Flow for Interposer Attach

In integrating this technology to the actual assembly flow of substrate-based devices, an interposer attach process is required on the assembly process flow shown in Fig. 5. It is worth to note that the assembly process flow varies with the product and the technology [1-2, 6-8].
In this process, an interposer bonder machine could be used as equipment to attach the interposer to the electrical layering of the substrate. The process starts by dispensing the conductive paste on top of the bond fingers in Fig. 6a then a bonder will attach the interposer on top of the conductive paste shown in Fig. 6b.

3.2 Wirebonding Process for Interposer

On a standard or typical process of wire bonding, a certain clearance is provided between bond fingers and die so that a good arching formation for the wire can be achieved [9,10], as shown in Fig. 7a. A closer distance between the die and bond fingers affects the consistency of the wirebonding process.

4. RESULTS AND DISCUSSION

With the integration of the electronic interposer design, the bonding pad for wirebond will be elevated. By increasing the height of the bond pad, the needed wire arching is reduced as well, eventually enabling a closer distance of wiring. Moreover, a shorter length of wire results to better structural stability for the wire making it more resistant to deformation or displacement during plastic encapsulation.

5. CONCLUSION AND RECOMMENDATIONS

The integration of electronic interposer in the current design of substrate-based product could benefit and address the current limitations of semiconductor electronic device assembly and could further improve its manufacturability and reliability performance. The improved design offers potential solution for the miniaturization of substrate-based product improving the current capability to process packages with tight clearance requirement.

Continuous process improvement and package design simulation and characterization are importantly helpful to sustain high quality

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES


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